NDnano Undergraduate Research Fellowship (NURF)
2015 Project Summary

1. Student name: Cleo Harvey

2. Faculty mentor name: Dr. Greg Snider

3. Project title: Ultra-low Energy Computation

4. Briefly describe any new skills you acquired during your summer research:

I gained a lot of new skills during my summer research in Notre Dame, and I was fortunate to have worked alongside highly skilled and experience scientists and engineering.

First of all, I was introduced to the clean room, in the Notre Dame Nanofabrication Facility (NDNF), where state of the art nanofabrication is performed in the Electrical Engineering building. The NDNF consists of three large areas: a class 10,000 area that houses Chemical Mechanical Processing, packaging and assembly, and Molecular Beam Epitaxy; and class 1000 and 100 areas that contain capabilities for metal deposition, lithography oxidation, dielectric deposition, plasma processing, and wet- chemical processing.
As a physics graduate, I was familiar with the basic operations of some of the equipment involved in IC chip fabrication, however this summer research gave me the opportunity to get some hands-on experience with world class equipment. I received training on and used the electron beam evaporator, the rapid thermal processing system, and the plasma-enhanced atomic layer deposition system for my work on investigating tunnel junctions in single electron transistors (SETs). In order to test the tunnel barrier materials, I became familiar with using a probe station, as well as a lock-in amplifier. I learned how to use L-Edit, a circuit layout editor, and acquired strong skills in chip design for my work with reversible computation.

5. Briefly share a practical application/end use of your research:

Scaling of traditional CMOS has been a huge advantage in recent years, making it possible for the electronics industry to maintain the expectations of device complexity set out by Moore's law. However, these advances will soon come to a halt due to limits in fabrication processes and sheer device complexity for example. Out of these many limitations, the most critical limitation has arguably been energy dissipation which is a consequence of current irreversible computing. Irreversible computation is governed by the erasure of bit information and according to Landauer's principle; a system that undergoes bit destruction will necessarily dissipate at least $k_B T \ln(2)$ Joules of energy.

To overcome this problem, the concept of reversible computing was proposed. The largest motivation for the study of technologies aimed at implementing reversible computing is that they offer what is predicted to be the only potential way to improve energy efficiency of computers beyond the fundamental limit of energy dissipation per irreversible bit operation. One proposed scheme for reversible computing is adiabatic switching and this is the scheme employed by Dr. Snider's group. By avoiding bit destruction in reversible adiabatic switching,

the bit energy is not dissipated into heat, and consequently, it is possible to achieve ultra-low power dissipation in computing.

Although my project title and work involved the circuit design of ultra-low energy computation, my time was also spent working with other graduate researchers in Dr. Sniders group. This work focuses on single electron transistors (SETs). These nanoscale electronic elements are capable of detecting the motion of individual electrons. Although SETs are unlikely to replace traditional FETs in applications, the main promising application for SETs is as efficient charge sensors for reading out spin or charge qubits confined in quantum dots. Other potential applications are supersensitive electrometers, single electron memory, and SET temperature standards.

Begin two-paragraph project summary here (~ one type-written page) to describe problem and project goal and your activities / results:

The reversible computational circuits that I was involved in designing were based on a 22nm FDSOI (fully-depleted silicon-on-insulator) fabrication process. I was mainly involved in the circuit design that used adiabatic computation to recycle energy. This design implemented Bennett clocks to aid in this recycling of energy. During the summer, there were three circuit designs created and the largest design was an Arithmetic Logic Unit (ALU) which is the basic unit of CPUs.

The circuit designs were created in a layout editor, L-Edit from Tanner EDA. The circuits were developed based on fabrication design rules set for a 22nm process. Most of the design rules are limited by the resolution of the fabrication techniques used to produce the chips.

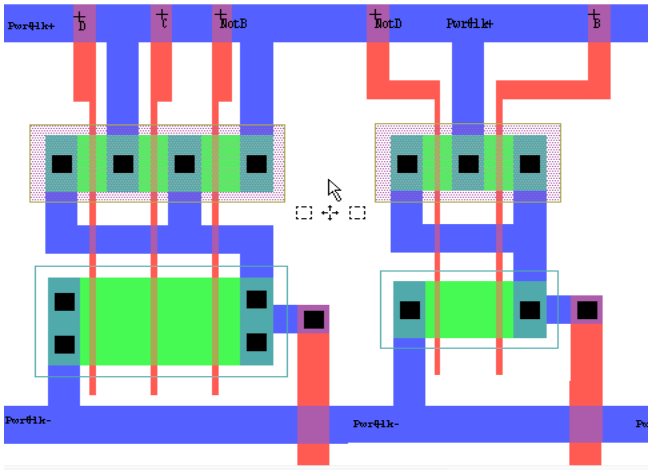

Figure 1. Sample of a 2input and 3input NAND logic gate for implemention in adiabatic circuits with 2 power clocks (PwrClk+ and PwrClk-)

I also worked on investigating tunnel junctions, which are the basic circuit element of single electron transistors (SETs). SETs take advantage of the Coulomb Blockade effect to control the flow of electrons and are made up of 2 tunnel junctions (source and drain) sharing a common electrode (called the island). Thus, to this extent the tunnel junctions behave in

principle like capacitors. Changing the voltage on the third gate junction affects the energy levels of the island. However, given that the dielectric is thin enough, the electrons from one electrode can tunnel through the dielectric to the next electrode.

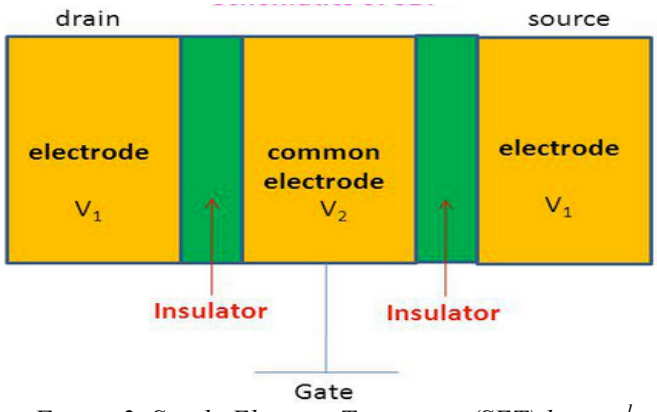

Figure 2. Single Electron Transistor (SET) layout.[1]

The tunnel barrier (dielectric) is very important. The charging energy E_c (the energy the electron needs to tunnel through the junction) is inversely proportional to the capacitance C. A sufficiently large charging energy (and voltage) is required for a tunneling event to be energetically favorable to occur. Due to the significant scaling of SET devices, there is a need for low-κ dielectrics to maintain a low capacitance and to increase the charging energy of the island.

The SET fabrication in Dr. Snider's group employs a thin film growth technique called Atomic Layer Deposition (ALD) to grow the tunnel barrier films. ALD is a very popular technique because of its ability to produce conformal high quality layers of material. ALD is based on alternating pulses of gas-phase chemicals called precursors. The precursors react with the substrate surface one at a time in a sequential self-limiting manner. Repeated exposures of the separate precursors, between purging steps, lead to an atomic layer-by-layer growth of film.

In support of the need for low-κ dielectrics as tunnel barriers, Silicon Nitride (SiN) was initially investigated as a possible candidate because its dielectric constant is comparable to SiO_2, which is heavily used as a low-κ dielectric. The use of SiN would also eliminate the problem of a Nickel Oxide layer forming at the junction, which occurs when using SiO_2. However, resistance measurements of ALD grown SiN sandwiched between layers of Nickel metal suggests that the ALD growth of SiN on Nickel is not "pinhole" free and thus unfavorable as a tunnel barrier in SETs.

The use of SiO_2 can still be favorable if the Nickel Oxide layers formed at each tunnel junction can be reduced. As a result of this, I focused on helping to investigate methods of reducing this oxide. This involved depositing a "blanket" layer of Nickel (50nm) on silicon wafer samples using the electron beam evaporator, which acts as the first electrode. The SiO_2 dielectric film was grown on top of the Nickel in the ALD system (~4nm). A stencil mask was used to deposit "dots" of (~60nm) Ni on top of the SiO2. Using these capacitor sandwich structures, the current through the structures were measured and thus the resistance was calculated. The samples were exposed to various reducing environments at different stages of fabricating the structure.

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[1] Norma L. Rangel Nanotechnology, Ellenbogen 2010

Measurements were performed with a lock-in amplifier connected to a pre-amp. Figure 3 below shows an example of the chance in resistance, hence conductance, of a particular sample after effective reducing of the Nickel Oxide.

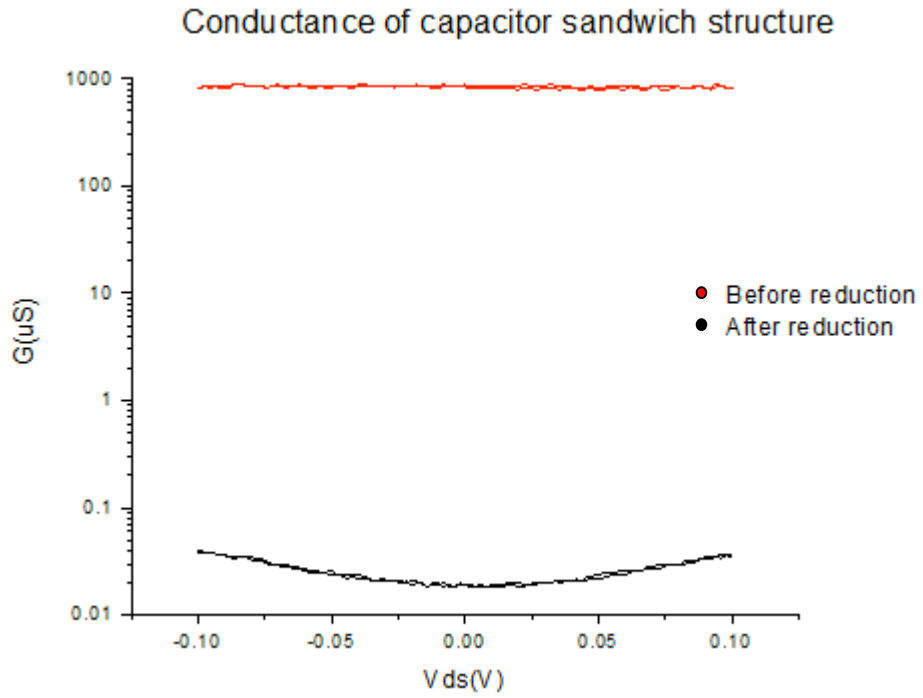

Figure 3. Effect of a reducing environment on the conductance of the capacitor structures. An increase in the conductance implies a reduction to the Nickel Oxide layer at each of the Nickel electrodes.