NDnano Undergraduate Research Fellowship (NURF)
2014 Project Summary

1. Student name: Xinyi Wang

2. Faculty mentor name: Patrick Fay

3. Project title: Design and Characterization of Ultrafast Chip-to-chip Interconnects

4. Briefly describe any new skills you acquired during your summer research: Simulation skills with the software HFSS; general knowledge of research process and methods; more in depth understanding of Coplanar Waveguide and transmission line;

5. Briefly share a practical application/end use of your research: Enhancing the performance of chip-to-chip interconnects could increase the frequencies of operation and bandwidth for electronics.

Project summary:

This research project is focused on enhancing the performance of Coplanar Waveguide (CPW) interconnect, which has operation frequency up to 200 GHz with Quilt Packaging technology [1]. The goal of the research is to test the Coplanar Waveguide interconnect performance for frequencies up to 750 GHz, and optimize CPW for higher operation frequencies.

To design and optimize CPW interconnects, the software HFSS is used for simulations. The project was started by replicating the simulations models from Qing Liu's dissertation paper on quilt packaging [1]. After obtaining satisfying results, basic enhancements were made according to technological progress in recent years. The substrate thickness was reduced from 600μm to 50μm; the chip-to-chip distance was reduced from 40μm to 10μm; wave port setup, instead of lumped port, was used for more accurate results at higher frequencies. In order to get a clearer understanding of the simulation results, straight through CPW models, instead of CPW interconnects, were simulated.

Several simulation attempts were made in order to develop CPW geometry with higher operation frequency. Substrate silicon with different resistivity was tested to find the most suitable material. Besides, according to the findings in the paper "Modeling Dispersion and Radiation Characteristics of Conductor-Backed CPW With Finite Ground Width", ground trace width of CPW can also affect its performance [2]. Therefore, simulations varying the ground width were made.

First, straight through CPW models with 10S/m and 0.01S/m silicon substrate were simulated. The following figure 1 shows the results of 10S/m silicon, and figure 2 shows the results of 0.01S/m silicon.

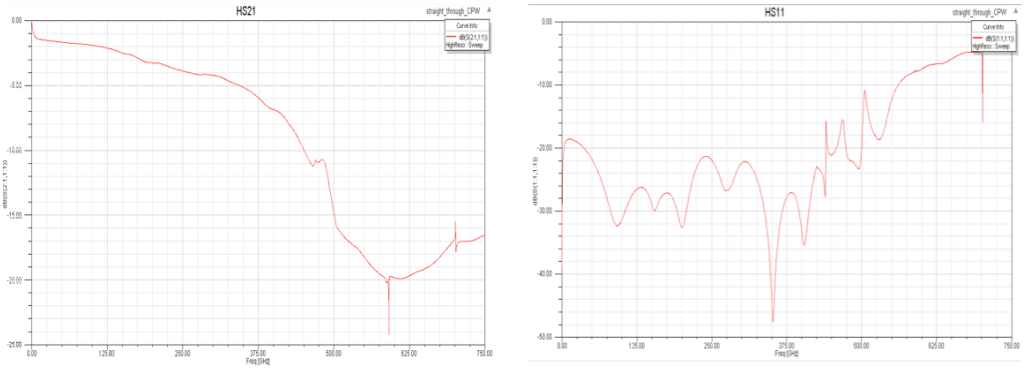

Figure 1. S21(left) and S11(right) of 10S/m silicon model

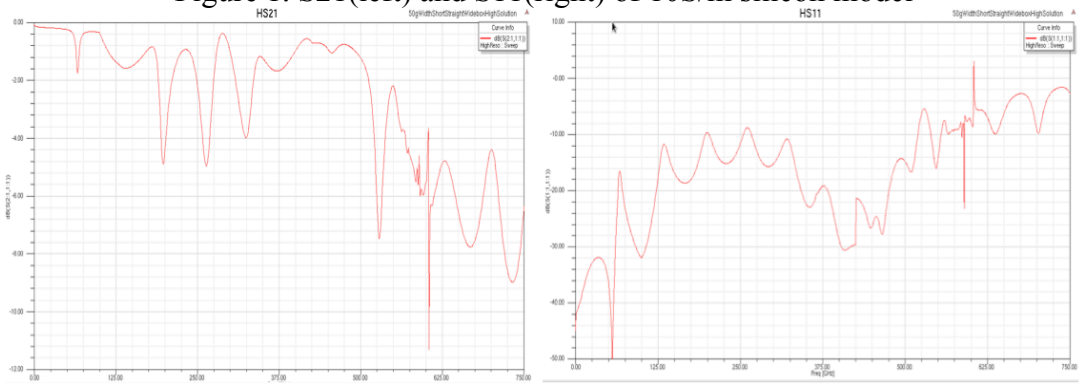

Figure 2. S21(left) and S11(right) of 0.01S/m silicon model

In figure 1 there is a steep slope at a very low frequency, although the S21 figure is quite smooth. This is probably because the loss due to a low resistive substrate covers up other more important problems. In figure 2, the huge slope problem is fixed, and only a huge “dip” occurs at around 65GHz. Therefore, high resistive silicon should be used for obtaining higher operation frequencies.

Second, a parametric setup was used to understand how ground width affect CPW performance. First, ground width was set to 30μm, 130μm, and 230μm. Figure 3 showed the results for this set of simulation.

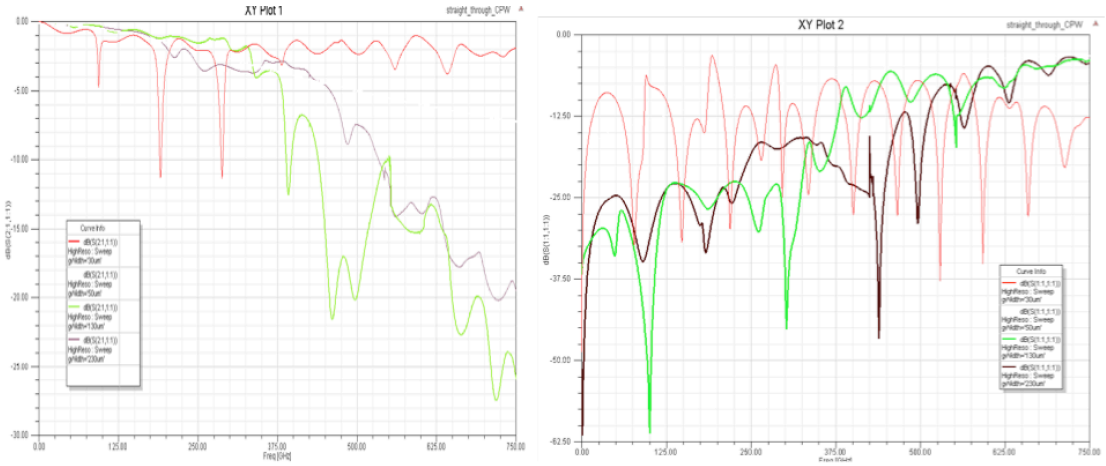

Figure 3. S21(left) and S11(right) for ground width parametric setup

In figure 3, red line represents ground width of 30μm, green line represents 130μm, and brown line represents 230μm. From the graph it is noticed that the CPW with 130μm ground

width has the widest bandwidth. Therefore, ground width is one of the parameters that can affect CPW performance. For a given CPW, simulations varying the ground width should be performed to get the range of values that has the best performance.

Future works and simulations could look into the specific relationship between ground width and CPW performance. More works are still needed to push the CPW operation frequency up to 500 GHz.

Works Cited:

[1] Qing, Liu, and Gary H. Bernstain. "QUILT PACKAGING: A NOVEL HIGH SPEED CHIP-TO-CHIP COMMUNICATION PARADIGM FOR SYSTEM-IN-PACKAGE." (2007): n. pag. Web. 15 June 2014.

[2] Schnieder, F., T. Tischler, and W. Heinrich. "Modeling Dispersion and Radiation Characteristics of Conductor-backed CPW with Finite Ground Width." *IEEE Transactions on Microwave Theory and Techniques* 51.1 (2003): 137-43. Web.