NDnano
Notre Dame Nanoscience and Technology

NDnano Summer Undergraduate Research
2021 Project Summary

1. Student name & home university: Abigail Brown, Saint Mary's College and University of Notre Dame

2. ND faculty name & department: Dr. Gregory Snider and Dr. Alexei Orlov, Electrical Engineering

3. Summer project title: Adiabatic capacitive logic for ultra-low power electronics

4. Briefly describe new skills you acquired during your summer research:

I had the opportunity to work in the nanofabrication facility, where I learned the mechanics of numerous machines. In the cleanroom, I acquired invaluable experience in many facets of integrated circuit production, primarily involving photolithography and dry etching, the key steps in modern microfabrication. I used the GCA Autostep 200 to selectively expose my silicon substrate to ultraviolet light to produce a desired pattern. Another machine that I used quite frequently was the RIE (Reactive Ion Etcher), which used specific gases to anisotropically etch materials. Outside the cleanroom, I gained insight about the responsibilities needed in order to function at a high-level professional environment

5. Briefly share a practical application/end use of your research:

Adiabatic Capacitive Logic is a future computing approach that could replace traditional CMOS circuits, in order to greatly reduce the heat dissipation in low power electronics.

6. 50- to 75-word abstract of your project:

Reversible computing is an approach that uses virtually adiabatic transitions and reversibility in order to mitigate heat dissipation. This is in a way similar to recycling of home waste – instead of throwing energy into heat adiabatic reversible logic aims at recycling energy. Implementations of reversible computing in modern CMOS circuits proved that there were still limits to the passive power dissipation. Adiabatic Capacitive Logic (ACL) is a possible implementation of reversible computing that uses variable capacitors in pull-up and pull-down networks that isn't limited to passive power and can recover 99.1% of its energy usage.

7. References for papers, posters, or presentations of your research:

[1] Celis-Cordova, Rene, Orlov, Alexei O, & Snider, Gregory L. (2020). *Adiabatic Capacitive Logic and the Limits of Adiabatic CMOS.*

One-page project summary that describes problem, project goal and your activities / results:

CMOS circuits use transistors to implement digital logic gates and to switch between on and off states. In every switching event, energy is dissipated as heat from the transistors. This heat dissipation limits modern computing. A favorable approach to energy saving computing is reversible computing, which lessens energy dissipation by using virtually adiabatic transitions and reversibility. An implementation of reversible computing is found in adiabatic CMOS circuits. However, these adiabatic CMOS circuits establish a trade-off between energy and speed. As the operating frequency reduces, the dissipation decreases until it reaches a limit of 3 MHz. The dissipation is no longer reduced after this, and passive power is the now main limitation of adiabatic CMOS circuits.

The goal of my project was to fabricate a device to limit this heat dissipation with the nascent approach of Adiabatic Capacitive Logic (ACL). ACL uses variable capacitors in pull-up and pull-down networks to implement reversible computing. Digital logic gates are created with ACL and function adiabatically by using a ramping voltage supply, as in adiabatic CMOS. In order to implement this, gap closing voltage-controlled variable capacitors were used, as they resemble micro-electromechanical system relays, and the degradation of the capacitors can be avoided.

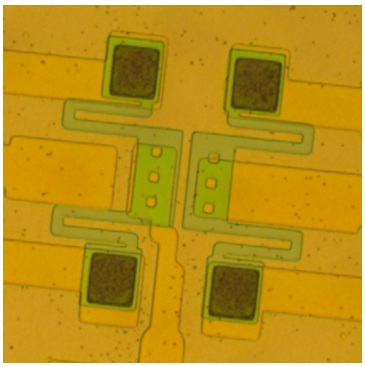

Figure 1: Top view of a partially fabricated ACL device

In order to create the device, I was to be trained in the cleanroom on numerous machines and to learn the different methods of IC fabrication. In the preliminary weeks, I was given two silicon wafers to practice photolithography, deposition, and etching. When I exhibited that I was proficient in using the machinery to perform the aforementioned tasks, I was given silicon wafers with LPCVD silicon nitride as a base insulator and titanium nitride as the base for the bottom electrodes. The first step was to complete the first lithography that outlined the electrodes. All of the lithography in this project utilized a GCA Autostep 200 to expose UV light through a reticle onto the substrate to create the dye that was desired. After the first lithography was complete, the RIE etched the titanium nitride electrodes, and cleaned using EKC265. Silicon dioxide was deposited, and the second lithography created the opening of the cantilever of the device. The silicon dioxide was etched with the RIE, the photoresist was ashed with the PVA, and the substrate was cleaned once again. Highly doped polysilicon was deposited to produce the cantilever, and a third lithography, etch, and cleaning were applied to that layer.

This device has yet to be completely fabricated. The future steps are to deposit undoped poly, complete the last lithography, etch, and cleaning, and to release this device using vapor HF. We will then run experiments on the working device to prove that it dissipates less energy than adiabatic CMOS circuits.