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Notre Dame Nanoscience and Technology

NDnano Summer Undergraduate Research
2021 Project Summary

1. Student name & home university:
Jacob Gose, University of Notre Dame

2. ND faculty name & department:
Prof. Gregory Snider, Prof. Alexei Orlov, Department of Electrical Engineering

3. Summer project title:
Adiabatic capacitive logic for ultra-low power electronics

4. Briefly describe new skills you acquired during your summer research:
Usage of various fabrication techonologies, including:

- Plasma-Enhanced Chemical Vapor Deposition (PECVD)
- Stepper Photolithography
- Anisotropic selective etching systems (i.e. Reactive Ion Etching)
- Imaging systems (i.e. Profilometers)

5. Briefly share a practical application/end use of your research:
Variable capacitor networks that perform logic functions in computers, like transistors, but dissipate very little energy to heat, and suffer very little mechanical degradation over time

6. 50- to 75-word abstract of your project:
The speed at which current logic devices, such as CMOS transistors, operate is limited by heat dissipation. Possible solutions studied include new types of operation, such as adiabatic CMOS, and devices, such as microelectronic mechanical structures (MEMS). Adiabatic capacitive logic combines principles of other solutions into a novel approach for creating ultra-low power electronics, based off variable capacitor networks. This project focused on the fabrication of such devices.

7. References for papers, posters, or presentations of your research:

[1] H. Samaali et. al., “MEMS four-terminal variable capacitor for low power capacitive adiabatic logic with high logic state differentiation,” Nano Energy, Virtual, 2019.
[2] Waldrop, M. Mitchell. “The Chips Are down for Moore's Law.” *Nature News*, Nature Publishing Group, 9 Feb. 2016, www.nature.com/news/the-chips-are-down-for-moore-s-law-1.19338.
[3] R. Celis-Cordova, A. O. Orlov, G. L. Snider, T. Lu and J. M. Kulick, "Adiabatic Flip-Flop and SRAM Design for an Adiabatic Reversible Microprocessor," 2020 International Conference on Rebooting Computing (ICRC), 2020.
[4] R. Celis-Cordova, A. O. Orlov, G. L. Snider, “Adiabatic capacitive logic using voltage-controlled variable capacitors,” IEEE Silicon Nanoelectronics Workshop, Virtual, June 2020.

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One-page project summary that describes problem, project goal and your activities / results:

Computers are built of logic units, devices that can emit either a low or high signal based on the signal into a third terminal (the "gate"). Commonly, this function is performed by CMOS networks. **Figure 1** shows a CMOS inverter, with inherent parasitic capacitance C_0; when V_{in} is low (logic "0"), the voltage V_0 across C_0 is V_{CC}. When V_{in} is high (logic "1"), C_0 is grounded. Manipulation of such networks and their configurations are used throughout computing applications [1].

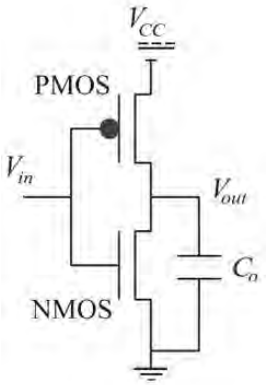

Figure 1. CMOS inverter with parasitic capacitance C_0

The number of CMOS transistors on a chip used to double every year, according to Moore's law, but this progress stopped due to quantum uncertainties at very fine sizes [2]. Focus was shifted to making individual CMOS transistors run faster. However, energy used to switch the voltage V_{in} is lost as heat, and if ran too quickly the transistor may become damaged or melt. This is the "active" energy loss. Moreover, some "leakage" current will flow through "OFF" transistors, incurring an additional "passive" energy loss. Recent research has been focused on remedying these problems.

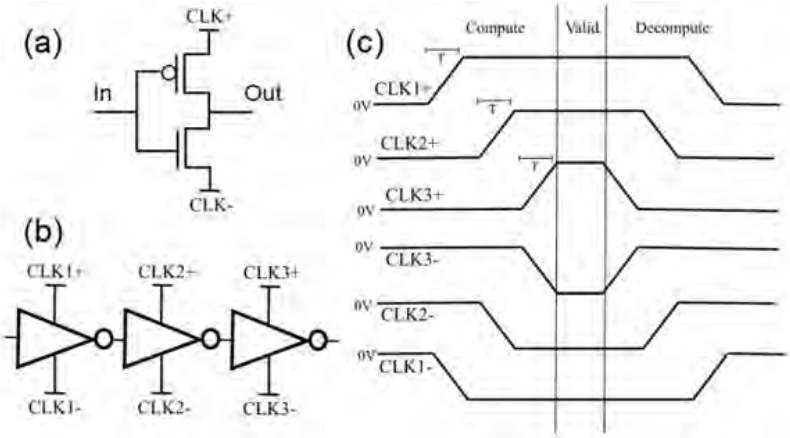

Figure 2. (a) CMOS inverter with Bennett "power" clocks (b) CMOS inverters in series, with different clocks (c) Bennett clocking signals (adiabatic operation)

Adiabatic CMOS addresses active energy loss by running CMOS transistors quasi-adiabatically. Instead of constant V_{CC} and GND signals, adiabatic CMOS uses ramped voltages. Sequences of devices are run in a scheme called "Bennet clocking", shown in **Figure 2** [3]. The ramping time of the voltage means an inherent reduction of speed, although regular CMOS is not run at its theoretical maximum anyway. This operation allows much of the energy used in switching to be recovered, mitigating the active loss. However, adiabatic CMOS still suffers from passive energy loss.

Microelectronic mechanical structures (MEMS) address passive energy loss by physically disconnecting terminals of OFF devices. Without a physical connection, there will be no electrical connection, so there is no leakage current. However, due to frequent physical connecting and disconnecting, MEMS often deteriorate rapidly, and are rendered unusable in a much shorter time than is expected for a logic device.

Adiabatic capacitive logic (ACL) devices are MEMS that, being capacitors, never physically connects their terminals. **Figure 3** shows a cross-sectional view of a gap-closing ACL structure, and **Figure 4** shows a top view [4]. The two parts of the structure are electrically isolated but mechanically connected, so the relative gaps between the parts of the device change if a voltage is applied to V_{in}, which changes the relative capacitances. Such variable capacitors can be implemented in CMOS-like networks to implement digital logic. Unlike other MEMS, the gaps are never totally "closed", so deterioration happens at a much slower rate.

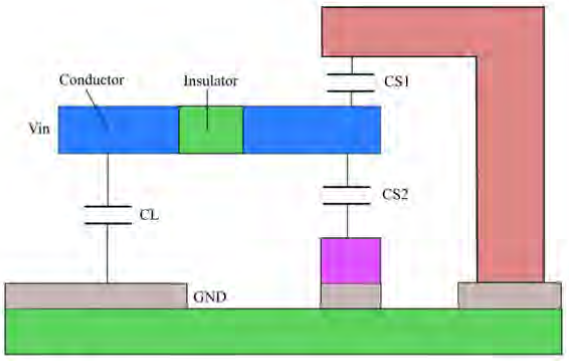

Figure 3. Cross-sectional view of ACL device

ACL devices can save monumental amounts of energy compared to similar devices. Since there is no physical connection between terminals, the device suffers no leakage current, eliminating passive energy loss. Additionally, simulations show, if run quasi-adiabatically, ACL devices can recover up to 99.1% of energy transferred, immensely reducing the active energy loss [4].

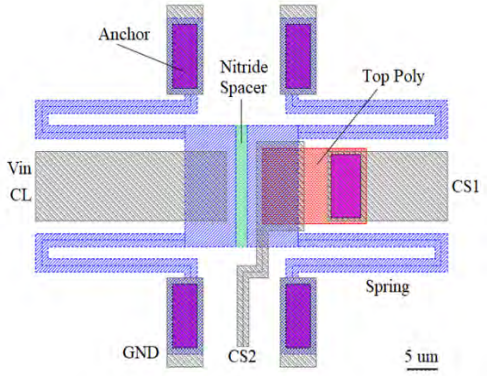

Figure 4. Top view of ACL device

This project was focused on fabrication of these devices. In a cyclical process of deposition-lithography-etching, thousands of different designs of ACL devices were fabricated on silicon wafers. The development of a design through the process is shown in **Figure 5.** The spacer physically connecting the two parts of the cantilever was planned to be silicon nitride, but instead undoped polysilicon was used. A layer of silicon dioxide underneath the cantilevers must be released before the devices are tested, but preliminary measurements so far have been promising. ACL has great potential for the future of low-power computing; this project is only the first step in that process.

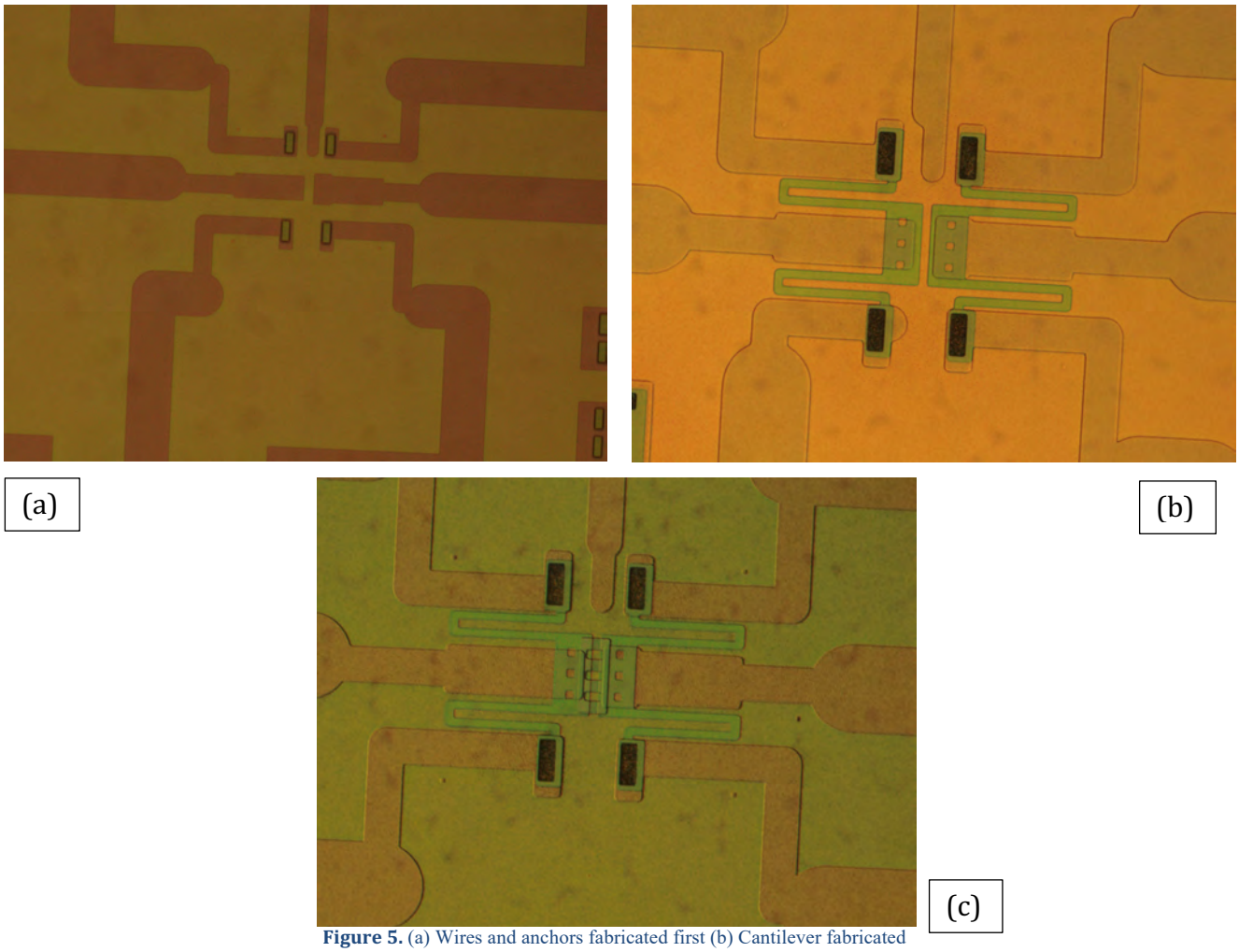

Figure 5. (a) Wires and anchors fabricated first (b) Cantilever fabricated resting on anchors (c) Spacer connecting two cantilevers