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Notre Dame Nanoscience and Technology

NDnano Summer Undergraduate Research
2022 Project Summary

1. Student name & home university:
Moboluwagbe Adesanmi, Villanova University

2. ND faculty name & department:
Dr. Gregory Snider, Dr. Alexei Orlov, Department of Electrical Engineering

3. Summer project title:
Single Electron Transistors (SETs) on SiN membranes for measuring Quantum Dots

4. Briefly describe new skills you acquired during your summer research:

I learned about the theory of SET device operation, how they are fabricated, and how to measure them using a probe station at room temperature and a cryostat at low temperatures. To make the SiN membranes, I learned to use photolithography and wet and dry etching, which are key steps in modern microfabrication. I also gained experience troubleshooting issues with the fabrication process. To use the switch matrix, a custom-built device for measure SETs, I learned about hardware and software debugging. I built one of the printed circuit boards and programmed a graphical user interface to control the switch matrix and organize the data it collected.

5. Briefly share a practical application/end use of your research:

Scanning probe microscopy systems that use single electron transistors (SETs) would be the most sensitive of known charge detection methods combined with a scanned-probe system. This project aims to use SETs to measure quantum electron droplets (QEDs) which have applications in quantum computing. SETs may be used for other nanoscale charge and voltage sensing applications in different sensors [1] and readout devices for quantum computers or in molecular computing.

6. 50- to 75-word abstract of your project:

SETs are the most sensitive charge detectors demonstrated to date. Scanning SET methods are intended for use to measure composite fermion and Majorana zero mode states in quantum electron droplets (QEDs) which could be useful for the realization of fault tolerant topological quantum computing. An SET based scanning probe system can be implemented by fabricating SETs on a silicon nitride (SiN) membrane to be used as a probe tip for an atomic force microscope.

7. References for papers, posters, or presentations of your research:

[1] Zirkle, Thomas A. A Parallel Single-Electron Box Array Scanning Probe. 2019. University of Notre Dame, PhD dissertation.

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One-page project summary that describes problem, project goal and your activities / results:

Single electron transistors (SETs) have the highest charge sensitivity of known detection methods, and can be used to measure individual electrons, making them very useful as electrometers. This has led to the development of SET based scanning probe systems. Scanning SET methods are currently intended for use to measure composite fermion and Majorana zero mode states in quantum electron droplets (QEDs) which could be useful for the realization of fault tolerant topological quantum computing. One possible implementation of an SET based scanning probe system involves fabricating a probe tip composed of SETs on a silicon nitride (SiN) membrane to be used with an atomic force microscope.

An SET has three terminals: a source, drain and gate. Electrons tunnel from the source to an island through a tunnel junction, which is an insulating barrier. At low temperatures, the voltage applied to the gate controls the movement of electrons onto the island by changing the island potential, resulting in periodic oscillations of conductance known as Coulomb oscillations.

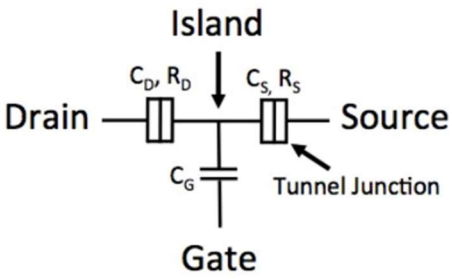

Figure 1: SET schematic

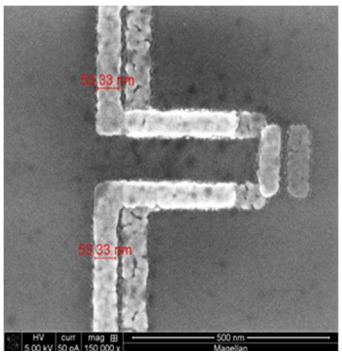

Figure 2: SEM of an SET on SiO_2

Figure 3: SiN membrane (green)

To form the membrane, 300 nm of SiN is deposited on a silicon wafer, and then the wafer is etched away from the back in areas patterned using photolithography. A finished sample is shown in the left figure where the green areas are the SiN membrane. SETs were fabricated on a separate die using electron beam lithography. Aluminum was deposited and oxidized in the patterned areas using the Niemeyer-Dolan technique of shadow evaporation. The source, drain and gate electrodes were made of aluminum, and the tunnel junctions were made of aluminum oxide.

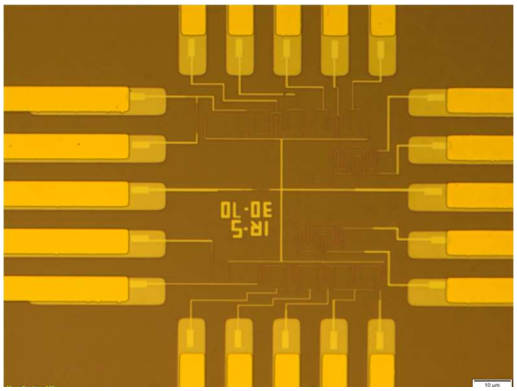

Figure 4: a single die with hundreds of SETs. Each finished SiO_2 chip had 16 of these die.

Each finished SET sample had 16 die, with each die having 20 pads leading to hundreds of SETs, so that manual measurement of each SET was a very time intensive task. The SETs are first tested at room temperature, where they are expected to behave like high resistance devices. There are "wires", i.e. continuous conductors for which the expected resistance must be R= Ro*l/S. There are also double tunnel junctions which can be quantified as either below or above a threshold resistance (~h/e^2=25.4 kOhm per junction). The ones below this threshold will not be able to fully develop Coulomb blockade conditions as electrons cannot be localized on the island. SETs that show resistance values above the threshold are then bonded and placed in a cryostat for measurements at temperatures as low as 4K. The conductance of the devices is measured for varying values of the source to drain voltage and the gate voltage.

A system was set up to automate room temperature measurements using a computer-controlled custom built switch matrix that reduces device testing time significantly. Software was developed which used the switch matrix, a lock in amplifier, and probe card to measure the SETs placed in the probe station. A measurement control file is sent as an input to the software. The software then updates the file with the requested measurements. and the final measurement output of the program is an average of several measurements, with the number of measurements and delay time between each measurement specified by the user. This way, the effect of background noise from transient voltages is reduced.

A spreadsheet template was also created to perform statistical analysis on the measurements from the switch matrix. The spreadsheet calculates the distribution of device resistance across the different die on a chip, displays this information with bar charts, and highlights devices that show resistance above the desired threshold value. With this, it is possible to select devices suitable for SET characterization, as well as investigate the effects of different changes to the fabrication recipes such as the quality of metallization, or oxidation.

The thermal evaporator that is typically used for the aluminum deposition and oxidation was recently repaired. Since this repair, the yield of SETs has been significantly lower. In the best chip, 12.5% of devices showed the expected resistance at room temperature. Three such devices have been measured at low temperatures and they show the expected relationship between the conductance, source to drain voltage and gate voltage. Once the fabrication processes for the SETs has been adjusted to increase the yield, SETs can be fabricated on the SiN membranes, and a scanning SET system can be implemented to measure QEDs.

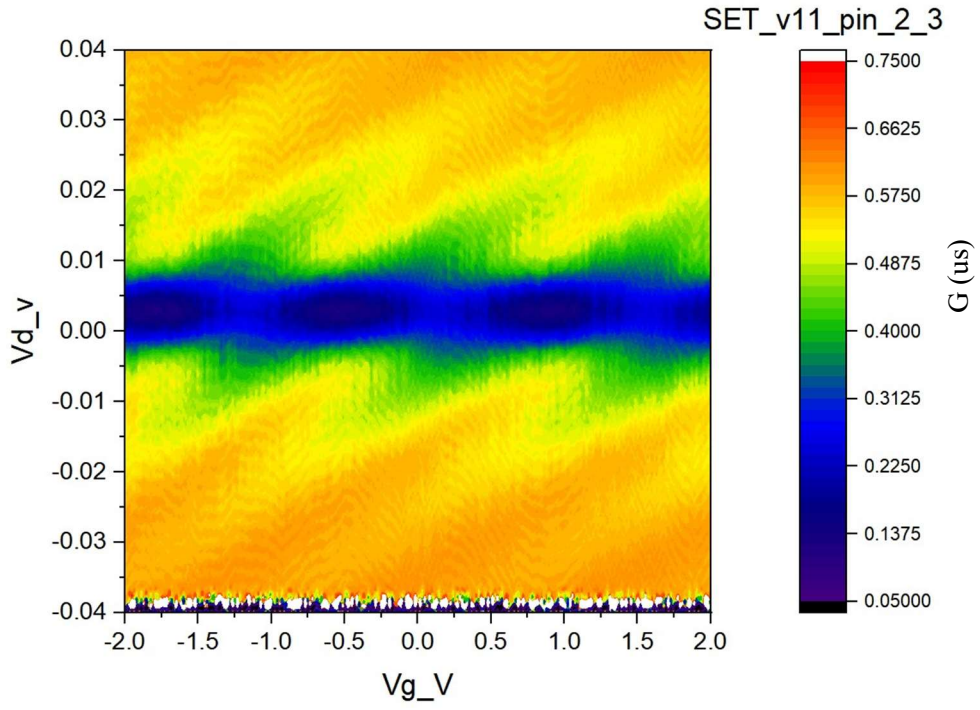

Figure 5: 4.1K measurements of conductance, “G” of one of the working SETs at different values of source-drain voltage, “Vd”, and gate voltage, “Vg”, showing the expected Coulomb oscillations.