NDnano
Notre Dame Nanoscience and Technology

NDnano Summer Undergraduate Research
2022 Project Summary

1. Student name & home university: Abigail Brown, Saint Mary's College and University of Notre Dame

2. ND faculty name & department: Dr. Gregory Snider and Dr. Alexei Orlov, Electrical Engineering

3. Summer project title: Adiabatic capacitive logic (ACL) for ultra-low power electronics

4. Briefly describe new skills you acquired during your summer research:

Since I have been continuing this research from last summer, I was able to explore and learn more in-depth procedures in the fabrication process. This summer, I was trained on two new machines used for fabrication. The first machine was the First Nano low pressure chemical vapor deposition (LPCVD) system, which uses low pressure, high temperature, and a mix of gasses to deposit polysilicon. The next machine I was newly trained on was the Thermco Furnace, which uses high temperature and a mix of gasses to dope polysilicon to make it more conductive for our devices. Because I was experienced with most of the machines used in the fabrication of the devices, I was able to learn more of the physics and theory behind how the machines work, and how our proposed ACL devices work. I also collaborated more on logistics of the fabrication with the graduate student I worked with to figure out etch times, and solutions to problems. With this, I also had independence in the cleanroom with the fabrication in some steps. Outside of the cleanroom, I learned how to better convey results succinctly and ask thoughtful questions when in an academic environment.

5. Briefly share a practical application/end use of your research:

Adiabatic capacitive logic can be used to construct and operate digital logic gates quasi-adiabatically. This allows for energy recovery in the system and can be used to dissipate less heat than conventional CMOS technology.

6. 50- to 75-word abstract of your project:

Conventional CMOS technology speeds are ultimately limited by heat dissipation. Adiabatic CMOS operations have been implemented to mitigate this dissipation, but it is limited by passive power dissipation caused by unavoidable leakage current. Adiabatic capacitive logic (ACL) utilizes variable capacitors to eliminate leakage current. By switching circuits quasi-adiabatically (by using linear ramps with a raise/drop time that is larger than its intrinsic RC time constant), the active power can be reduced, and less heat is dissipated with energy savings up to 50%. Even greater reduction in power dissipation can be achieved by using reversible computing.

7. References for papers, posters, or presentations of your research:

[1] Celis-Cordova, Rene, Orlov, Alexei O, & Snider, Gregory L. (2020). *Adiabatic Capacitive Logic and the Limits of Adiabatic CMOS.*
[2] R. Celis-Cordova, A. O. Orlov, G. L. Snider, "Adiabatic capacitive logic using voltage-controlled variable capacitors," IEEE Silicon Nanoelectronics Workshop, Virtual, June 2020.

One-page project summary that describes problem, project goal and your activities / results:

CMOS field-effect transistors are used as switches and are essential for processing instructions inside a computer. This technology used to follow Moore's law, that states the number of transistors double every year and the speed at which they run at also increase. The problem with Moore's law in current technology is that the speed that the transistors are ran at has plateaued. This is because energy dissipates as heat when transistors are run at speeds on gigahertz order. The current that the devices leak is due to the quantum tunneling of the electrons through the CMOS gates. When electrons tunnel through at these speeds, transistors can melt, and information can be lost. Adiabatic CMOS operations have been adapted to mitigate this problem but is ultimately limited by the passive energy loss.

Adiabatic capacitive logic (ACL) implements reversible computing by using variable capacitors in pull-up and pull-down networks. ACL eliminates leakage current since there is no contact between the cantilever and the bottom electrode and therefore the device is not limited by passive power. ACL is implemented through micro electrical mechanical systems (MEMS). Reversible computing reduces heat generation by avoiding unnecessary dissipation and introduces a trade-off between energy and speed. By switching the circuits at a time that is much greater than the respective RC time constant, active power can be drastically reduced. This is implemented in our project using ramping clocks in place of DC power supplies to operate them quasi-adiabatically, or without heat transfer.

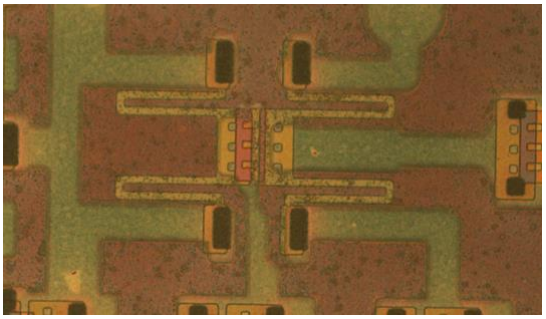

Figure 1: Top view of an unreleased device

When the devices were first fabricated in the cleanroom, we used a silicon substrate. When those devices were complete and tested, it was found that the silicon introduced this parasitic capacitance that created background noise that made it difficult to measure the devices correctly. To mitigate this, insulating fused silica ("quartz") substrates were used to eliminate parasitic capacitance and to eliminate substrate conductance. Fabrication involved cyclical processes of deposition, patterning, and etching. Titanium nitride was used to create the electrodes. Silicon dioxide was used as a sacrificial layer to hold the cantilever until release. Polysilicon was used for the cantilever and further doped to increase conductivity. An undoped polysilicon spacer was implemented to electrically isolate the capacitors. To complete the devices, a vapor HF system is used to remove the silicon dioxide.

More devices are being tested and fabricated to get better results. Additionally, with simulations, it was found that 99.1% of energy can be recovered if ACL and reversible computing are used concurrently. Future fabrication plans include depositing gold on the titanium nitride pads to further reduce the parasitic series resistance and depositing an additional doped polysilicon spacer to be able to cascade the devices.