NDnano
Notre Dame Nanoscience and Technology

NDnano Summer Undergraduate Research
2023 Project Summary

1. Student name & home university: Daniel Noronha, University of Notre Dame

2. ND faculty name & department: Dr. Gregory Snider and Dr. Alexei Orlov, Electrical Engineering

3. Summer project title: Adiabatic Capacitive Logic & Clocking Systems for Ultra-Low Power Electronics

4. Briefly describe new skills you acquired during your summer research:

This summer, I developed my PCB design skills by designing (and assembling) multiple PCBs with surface mount (SMD) and through-hole components, including a 460-component motherboard to test our RH90 MIPS microprocessor's heat dissipation and functionality in adiabatic mode. I also learned to assemble surface-mount devices with solder paste and to use the manual pick-and-place machine in the EIH, as well as the solder reflow oven. I learned about the fundamentals of IC fabrication in the ND Nanofabrication facility (class 100 cleanroom) while fabricating AlN resonators which will form the clocking system for the ACL devices. This included wafer cleaving, sputtering Aluminum with the Oerlikon single-chamber sputtering system, SPR-700 photoresist spinning, lithography (UV exposure) in the Autostep 200 i-line stepper, development in AZ-917, etching Aluminum in the PlasmaTherm 790 Reactive Ion Etcher (RIE), and SiO2 deposition in the PECVD machine. Additionally, I used a probe station, optical microscopes, ellipsometer, and stylus profilometer to characterize my samples at various stage of the fabrication process.

5. Briefly share a practical application/end use of your research:

AlN resonators are a promising means of creating on-chip ramping power supplies that enable our ACL devices to run adiabatically. Adiabatic capacitive logic devices minimize heat dissipation by introducing a trade-off between speed and power. Furthermore, reversible digital logic gates can be constructed using ACL, allowing the devices to recycle energy so they dissipate less heat than traditional CMOS devices whose maximum operating frequencies and overall efficiency are now severely limited by their heat dissipation.

6. 50- to 75-word abstract of your project:

Adiabatic Capacitive Logic provides an alternative implementation of digital logic gates (to standard CMOS) by eliminating the issues of subthreshold leakage current in NMOS and PMOS transistors and minimizing heat dissipation from switching power supply clocks. This is achieved by using voltage-controlled variable capacitors implemented through MEMS (microelectromechanical structures) rather than MOSFETs, and by using linear ramping clocks in a Bennett clocking scheme (ramping time >> RC) with reversible logic rather than instantaneously switching clocks.

7. References for papers, posters, or presentations of your research:

- S. McConnell, M. (2018). *Adiabatic Reversible Computing: Measurement of Heat Dissipation Using Nanothermocouples and Fabrication of MEMS Power Clocks* [PhD Dissertation]. University of Notre Dame.
- Celis Cordova, R. (2022). *Reversible Computing: Adiabatic Capacitive Logic* [PhD Dissertation]. University of Notre Dame.

One-page project summary that describes problem, project goal and your activities / results:

Traditional CMOS technology is facing several issues with scaling in recent years as we approach the end of Moore's law. Although microprocessor manufacturers have found ways of improving performance of their latest chips every year, this has also come at the cost of an increased TDP (thermal design power), with the i9-10990XE for instance having an extremely high TDP of 380W! Moreover, microprocessor operating frequencies have also been limited to around 4GHz since 2004 even though their RC time constants are much lower.

Our project offers an alternative approach to digital logic in which ramping clocks are used rather than instantaneous ones. Instantaneous switching draws a lot of current, and thus power, during transitions as the switching time is much shorter than the RC time constant of the circuits (current draw is proportional to $e^{-t/RC}$ for transistor gate charging and discharging). Ramping clocks use a ramp time that is much longer than the RC time constant, which enables quasi-adiabatic transitions and introduces a tradeoff between speed and power that is useful in low-power electronics. Moreover, using a reversible Bennett clocking scheme with variable voltage-controlled MEMS capacitors allows energy to be recycled rather than dissipated as heat to the environment. This improves thermal efficiency and could ultimately even allow for operating frequencies above 10 GHz.

My research this summer focused on two major areas: designing and assembling PCBs to test our fabricated chips (designed in-house but sourced externally due to fabrication complexities), and fabricating Aluminum Nitride resonators to function as ramping clocking inputs to the microprocessor. The RH90 MIPS microprocessor we designed can run in both 'CMOS mode' and 'Adiabatic mode', allowing us to compare their heat dissipation when programmed to perform the same tasks through a Virtex-7 FPGA. I designed PCBs that allowed the FPGA to interface with the microprocessor (seated within an 88-pin socket) via a 400-pin FMC connector with active level shifting on all 16 bidirectional I/O pins to ensure that the FPGA logic levels (0-1.8V) match those of the MIPS microprocessor in Adiabatic mode (-0.6V-+0.6V) when reading and writing.

The Aluminum Nitride resonators I worked on consist of interdigitated fingers of Aluminum Nitride attached to Aluminum bond pads that are supported on two ends but are otherwise free to resonate (MEMS). This is possible because of the piezoelectric properties of Aluminum Nitride that allow it to resonate when a varying voltage is applied through an oscillator to maintain a stable clock. To fabricate these devices, I started with a ~600µm Silicon wafer with 1µm of Aluminum Nitride sputtered at Carnegie Mellon University. I sputtered 200nm of Aluminum (with 2% silicon) over 10 minutes on a cleaved sample after surface cleaning. I then treated the sample with HMDS for 2 minutes and spun SPR-700 photoresist for 30 seconds at 4000rpm, followed by a soft bake at 90°C for 1 minute. Next, I used the Autostep200 i-line stepper to expose my sample for 0.28 seconds and developed it in AZ-917 for 45 seconds. Finally, I etched the Aluminum to pattern my sample in the Reactive Ion Etcher, which also plasma-ashed the remaining photoresist and performed passivation steps. Figure 1 shows an optical micrograph of the structures (top view) at 5x/20x after etching/ashing, alongside a cross-section.

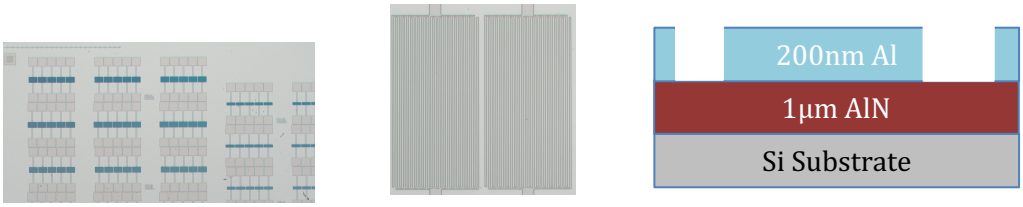

Figure 1. AlN resonators after etching at 5x (left) and 20x (middle), with associated cross-section (right)

My future work will involve further thermal testing of ACL devices after assembling the designed PCBs, and I will continue with further steps of AlN resonator fabrication such as etching the AlN through an SiO2 hard mask and etching the silicon substrate underneath the resonators with XeF_2 to release them.